

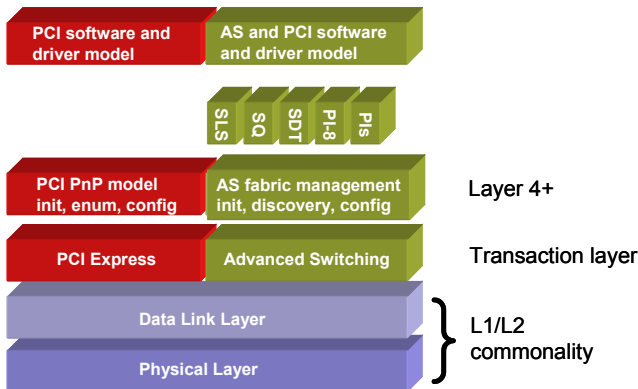
PCI-Xactor Test Environment

Your Proven Path to PCI Express and AS Compliance Validation



HIGHLIGHTS

- Complete solution to verify PCI Express, PCI-X, PCI 2.3 components and peripherals
- Complete solution to verify Advanced Switching components and peripherals including PI-8, Portal, SLS, SQ, SDT
- Comprehensive BFM support – Root Complex, Endpoint, Switch, Bridge
- Endpoint, Switch, Bridge testbench frameworks ease integration of DUV and running compliance testsuites
- Supports active test generation and passive SuperMonitor link monitoring
- Comes with compliance test suites based on PCISIG and ASISIG checklists and test specifications
- High-level PCI transaction API supports Verilog, SystemVerilog, Specman, Vera, C/C++, and VHDL
- Protocol verifiers check and reports all PCI Express/Advanced Switching/PCI-X/PCI compliance violations
- Functional coverage monitor reports device and command utilization



OVERVIEW

The PCI-Xactor test environment is a set of behavioral models (BFMs) and test suites that simulate the behavior of the PCI Express, Advanced Switching, and PCI-X links. The models, provided in Verilog HDL, are tools for system designers to exercise and debug the design of components/systems based on the all PCI and ASI standards – PCI Express, Advanced Switching (AS), PCI-X, and conventional PCI. Designs under verification (DUVs) can be verified against all realistic system topologies including bridge and switch-based topologies. The objective of the models is to aid in the functional verification process prior to silicon or board fabrication. The test environment, provided in Verilog, VHDL, SystemC, ANSI C/C++, SystemVerilog, Specman, and Vera, provides a high-level test API to interact with the behavioral models supporting AS nodes,

PCI Express root complexes, endpoints, switches and PCI-X/PCI 2.3 master and target devices, a PCI-X/PCI 2.3 arbiter to control bus access, and a SuperMonitor model which passively monitors and reports AS, PCI Express, PCI-X, PCI 2.3 protocol violations, validates end-to-end transactions, and measures and reports transaction trace analysis of devices by address, bytes transferred, and command types utilized. In addition, the test environment includes a full suite of compliance test scenarios that verify endpoint, switch, and bridge designs are comply fully with the AS, PCI Express, PCI-X and PCI 2.3 specifications.

Assertions

TXN.2.21#11	CHECKED
TXN.3.2#35	CHECKED
TXN.2.2#4	CHECKED
TXN.3.2#14	NA
...	
DLL.3.1#5	CHECKED
DLL.3.1#6	NA
DLL.4.1#2	CHECKED
DLL.4.1#7	ASSERTED
PHY.2.1#2	CHECKED
CFG.10.0#1	NA
CFG.8.5#3	NA
DLL.5.2#12	CHECKED

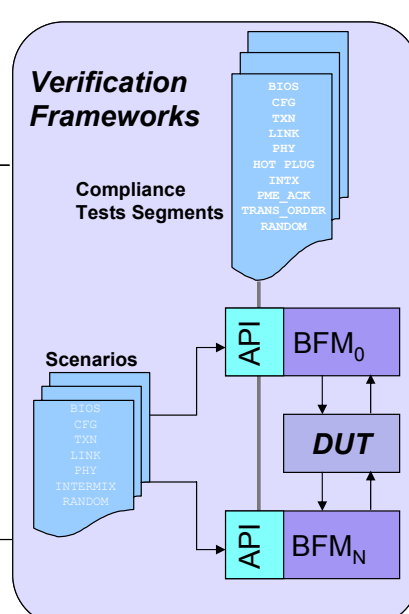
Checked items : 109 (25.41%)
Asserted items : 1 (0.23%)

Compliance Test Coverage

link_test111_2port	Index	Test Name	Result
	1	test111rc	FAILED
	2	test111ep	PASSED

link_test412_2port	Index	Test Name	Result
	1	test412rc	PASSED
	2	test412ep	PASSED

link_test5210_2port	Index	Test Name	Result
	1	test5210rc	FAILED
	2	test5210ep	FAILED



Enumeration Result

```
**** Enumeration Bus/Device/Function Map ****
B0 D0 F0 ROOT_COMPLEX global index 1 prefetch memory
the other side B1 D0 F0 SWITCH_UPSTREAM global index 2
B2 D1 F0 SWITCH_DOWNSTREAM global index 3 prefetch memory
the other side B3 D0 F0 ENDPOINT global index 4 prefetch memory
```

Symbol Tracker

TIME	RX1	EX1	RX2	TX2
3800	---	00	---	00
7800	---	COM	---	COM
11800	---	PAD	---	PAD
15800	---	PAD	---	PAD
16001	COM	---	COM	---
19800	---	0a	---	0a
20001	PAD	---	PAD	---
23800	---	02	---	02
24001	PAD	---	PAD	---
27800	---	00	---	00

Packet Tracker

START TIME	FINISH TIME	D	I	CREDITS	S
1734021	1738021	D	IFC2_CPL	0	0
1754001	1758001	U	IFC2_CPL	5	88
1742021	1766021	D	MSGD	---	000
1770021	1786021	D	CFG_RD_0	---	001
1930001	1934001	U	ACK	---	001
2026001	2030001	U	FC_P	6	89
2090001	2094001	U	FC_NP	10	9
2442001	2462001	U	CMPLT_D	---	000

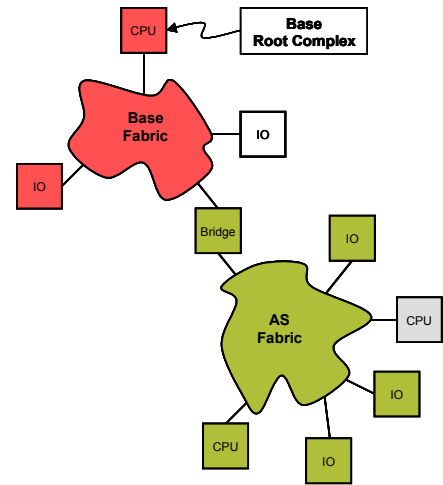
PROGRAMMING INTERFACE

The PCI-Xactor test environment supports a powerful transaction API for the development of diagnostic test programs and is written in native Verilog and SystemVerilog HDLs. Specman, Vera, VHDL, and C/C++ are supported through thin-client

call layers. This simple, well-defined test API enables application designers to create any combination of AS/PCI Express/PCI-X/PCI 2.3 transaction scenarios. From a single diagnostic test program, verification engineers can control multiple BFM, direct normal and error transactions, access test assertion databases, and write log files.

ENDPOINT AND SWITCH VERIFICATION FRAMEWORKS

The PCI-Xactor BFM's support AS, PCI Express, PCI-X and PCI 2.3 specifications. Complete endpoint and switch frameworks come configured to instantiate multiple BFM's including PCI Express root complex, endpoint, switch and PCI/PCI-X master and slave devices. DUV integration and device configuration is simplified through bios enumeration. Compliance tests can be reused by all configurations without modifications. Protocol checkers implement the PCISIG Checklists and report assertion violations and trigger coverage. Verification test writers have the ability to selectively randomize 100s of device behaviors (e.g., ACK/NAK response, lane-to-lane skew, DEVSEL timing, retries, disconnects, etc.) within the model for optimal test coverage under realistic conditions. The model can handle any type of split transaction scenario. Each BFM contains a complete PCI configuration space with parameterized base address registers to enable easy setup of custom system simulations. Auto-enumeration of the system topology is also supported to ensure DUTs adhere to legacy PCI 2.3 system software.



SUPERMONITOR TARGETS SWITCH AND BRIDGE VERIFICATION

During AS, PCI Express and PCI-X bus operation, the SuperMonitor detects endpoint, switch, and bridge protocol violations, measures link bandwidth for each request/completer pair, and measures functional coverage of AS and PCI command types, addressing, and PCI bus timing signals. The SuperMonitor records bus activity during the simulation to log files. The SuperMonitor also verifies end-to-end transactions to ensure transactions complete successfully. Specifically the end-to-end transaction checker is user-configurable to support any PCI system topology. A generic end-to-end checker is configured to verify: a) Termination conditions (normal, retry, split termination, error); b) Data integrity (byte count, parity, CRC); c) Data contents (expected memory, IO, and configuration register values); d) Transaction ordering rules (strict, relaxed). The SuperMonitor extensively utilizes TestWizard's transaction database functions to store and query split transaction completion transactions on one or more busses.

DEVICE UNDER TEST

The AS/PCI application designer can easily link the device under test into the test environment by instantiating the design description (RTL or gate level) into the test environment's top-level system test bench. The designer can then run the compliance suite included with the test environment, and can use the transaction API to create custom tests. DUT integration of the user-side logic is also supported enabling full control over the DUT to initiate transactions.

AS/PCI EXPRESS/PCI-X/PCI 2.3 COMPLIANCE TEST SUITE

The test environment includes a suite of functional compliance tests based on protocol scenarios outlined in the Checklists and Test Specifications provided by the PCI Special Interest Group (PCISIG) and Advanced Switching Special Interest Group (ASISIG) including: a) PCI Express endpoints, switch, and bridge; b) PCI-X master and slave tests; c) PCI 2.3 master and slave tests. Functional compliance test coverage and assertion/checklist coverage is also provided giving a formal measure of DUV compliance. Tests are highly reusable on any design/topology based on an innovative scenarios-based methodology. Random and directed testcases are supported. Tests can be randomized at the TL/DLL/PHY layers as well at the test segment and scenario-level.

PLATFORM SUPPORT

Solaris, Linux, Windows

SIMULATOR SUPPORT

Cadence	Verilog-XL	NC-SIM
Synopsys	VCS	
Model Technology	ModelSim	

LOCATIONS AND FACILITIES

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