USB-Xactor Test Environment

Your Solution to USB Compliance Validation

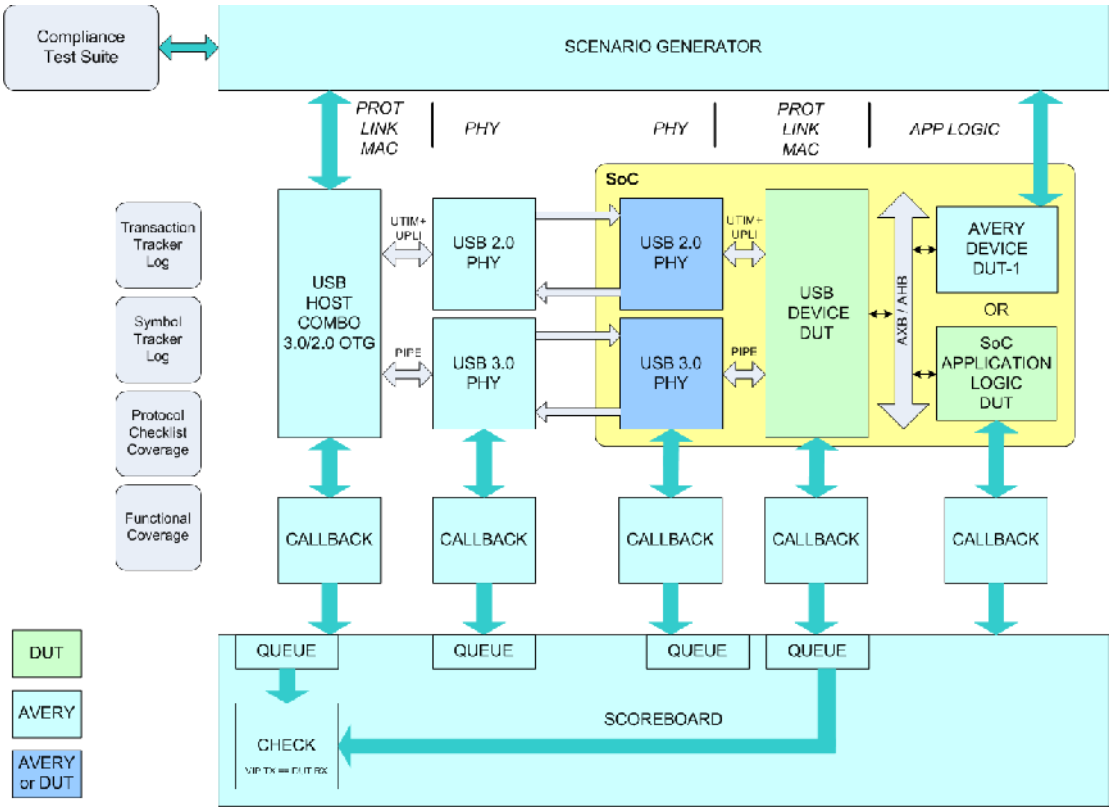
HIGHLIGHTS

- Complete solution for USB 2.0, OTG, and 3.0 core through chip-level verification
- Host, Device, Hub, PIPE/PHY models
- Compliance testsuite for Protocol, Link, and Physical layer verification of Host, Device, Hub, PHY
- Comprehensive assertions track USB compliance coverage
- Functional coverage tracks range of packet traffic, FSMs, and complex operational sequences
- Packet and symbol tracker monitor output improves debug
- Supports Verilog and SystemVerilog OVM/VMM environments
- Delivered in SystemVerilog source code
- Proven with multiple IP vendors

INTRODUCTION

The USB-Xactor supports verification of USB-based designs using the USB 2.0 and 3.0 standards. USB-Xactor allows users to verify their designs by developing custom tests at several levels of abstraction. USB-Xactor models support APIs from the pseudo USB Driver (USBD) and Host Controller Driver levels down to interacting directly at the protocol through physical layers. Major features supported are:

- Host performs bus enumeration and and allocates independent USB pipes for communication flows between host and each device endpoint
- Program TP sequences for Bulk, Isochronous, Interrupt, Bulk Stream, and Control transfer types
- Program USB Device requests to access USB device descriptors
- Automatic frame scheduling and bus interval and service interval support including ITP generation
- Program host and device model timing parameters and response behaviors such as link commands
- Fine-grained control over LTSSM transition sequences
- Fine-grained link layer controls
- Inject errors at all layers through callbacks
- Control device operations state transitions including suspend/resume
- Full power management support (U0-U3) including automatic and software directed entry/exit
- PowerOn and Inband reset



SYSTEMVERILOG ENVIRONMENT

USB-Xactor supports an object oriented SystemVerilog testbench

- VMM and OVM support
- Abstract data model for transfer, packet, and descriptor types
- Drivers, event callbacks, and scoreboard options to automate status and result checking
- Directed and random error injection supported through callbacks and built-in methods
- Random scenario generation with constraints stress design operation
- Directed tests for focused functional compliance testing
- Functional coverage monitoring of scenario cases
- Comprehensive protocol checking
- Packet and symbol tracking log files

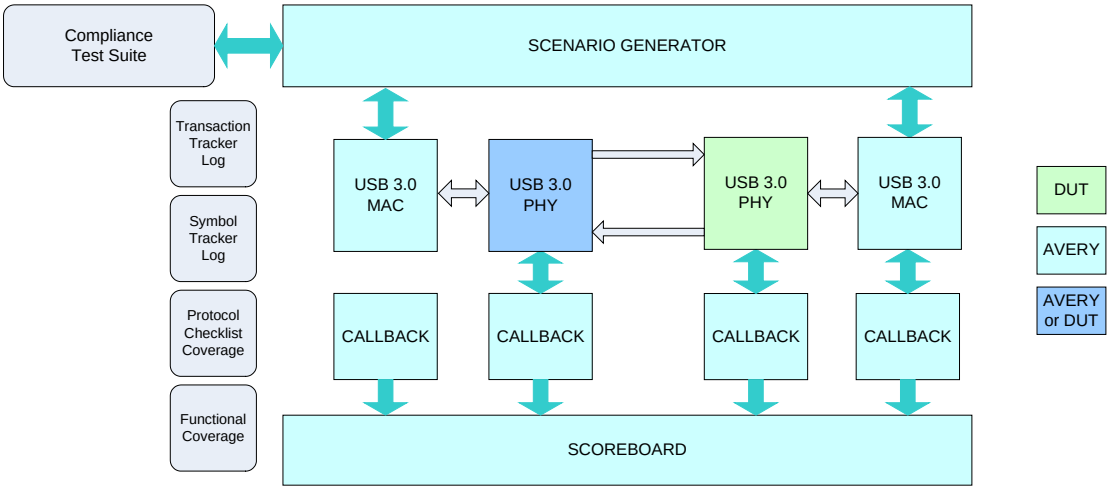
CORE THROUGH CHIP-LEVEL VERIFICATION

The USB application designer can easily link the device under test into the test environment including DUT integration of the user-side logic to an USB-Xactor protocol layer model enabling full control over the DUT to initiate transactions via HCDI operations. Device and PHY-only core verification is supported.

```
==> 2826119 AUSB_DP(Setup) 48c20f48 00088000 00005817
    |address      |route                                  |typ      |
    |24___________|6107a____________________________________|08_______|
    |dataLength                    |s|rsvd1|eptNum |d|e|r|seqNum   |
    |0008__________________________|1|0____|0______|0|0|0|00_______|
    |rsvd2_1|p|rsvd2_0             |streamId                       |
    |0______|0|000_________________|5817___________________________|
    link control: crc=07 deferred=0 delayed=0 hub_depth=0 seq=4
    80 06 00 01 00 00 00 02
<== 2896123 AUSB_TP(AUSB_TP_ACK) 48c20f44 00208001 00005817
    |address      |route                                  |typ      |
    |24___________|6107a____________________________________|04_______|
    |rsvd1_2    |seqNum   |numP     |h|rsvd1|eptNum |d|r|rsv|subType|
    |00_________|01_______|00_______|1|0____|0______|0|0|0__|1______|
    |rsvd2_1|p|rsvd2_0             |streamId                       |
    |0______|0|000_________________|5817___________________________|
    link control: crc=13 deferred=0 delayed=0 hub_depth=0 seq=5
```

COMPLIANCE TEST SUITE

The test environment includes a suite of functional compliance tests. Random and directed testcases are supported. Random testing supports generating random USB transfer types and PROTOCOL/LINK/PHY layer behaviors including error injection.



USB PIPE PHY Core Testbench

PLATFORM SUPPORT

Solaris, Linux, Windows

SIMULATOR SUPPORT

Cadence NC-SIM, Synopsys VCS, Mentor Questa

LOCATIONS AND FACILITIES

U.S. Headquarters: 2 Atwood Lane, Andover, MA 01810, Tel: 978 689 7286, Fax: 866 457 1388
International Field Office: 76, 1st Section, Chung-Hsiao E. Rd., suite 1203, Taipei, Taiwan, ROC, Tel +886-2-23278766

Sales

Avery Sales and Support	978 689 7286	Worldwide
Saphirus	408 625 7618	(US West)
BlackForest EDA (blackforest-eda.de)	+49-2132-137485	(Europe)

WEBSITE: http://www.avery-design.com